REMARKS

Claims 1-26 and 49-57 are currently in the application for further prosecution. By this amendment, Claims 1, 2, 5-7, 9, 12, 14, 16-19, 49, 51, and 55-57 have been amended.

Procedural Objections

The Office Action has rejected the long IDS previously filed because there is no explanation of the foreign references. According to MPEP section 609.04(a), the duty of candor does not require that the applicant translate every foreign reference. Applicant is not attempting to mislead the Office in submitting the translation of the abstract for the foreign references. The translation of the abstract is sufficient for the consideration of the entire reference as "submission of an English language abstract of a reference may fulfill the requirement for a concise explanation." MPEP section 609.04(a)(III). Applicant respectfully requests consideration of the entirety of the foreign references previously submitted based on the abstracts.

The Office Action has also noted that some of the cited references in the IDS are in unrelated field and are therefore incorrectly cited. The Office Action has not indicated which references are incorrectly cited. Applicant respectfully requests that the Office identify the cited references that the Office Action asserts are incorrectly cited.

The Office Action has objected to claim 49 for an informality based on a repeated comma. Applicant has amended claim 49 to correct this noted error.

Claim Rejections § 103

Claims 1, 7-11, 13-15, 21-26, 49 and 52-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,142,731 ("Toi") in view of U.S. Patent No. 5,956,518 ("DeHon"). The Office Action has noted that the phrase "capable of" is non-limiting and therefore has not been given patentable weight. Applicant has amended the claims to eliminate

this phrase and therefore requests that such elements previously modified by the phrase "capable of" in the claims be given patentable weight.

Claims 2-6, 12 and 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toi and DeHon and further in view of U.S. Patent No. 6,778,212 ("Deng").

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toi in view of DeHon and further in view of U.S. Patent No. 5,754,227 ("Fukuoka").

The present invention relates to image processing systems that take advantage of the use of heterogeneous computational units composed of multiple computational elements that may be rapidly reconfigured via an interconnection network. The Office Action acknowledges that Toi does not disclose heterogeneous computational elements or an interconnection network. (p. 8). The Office Action has combined Toi with DeHon which allegedly discloses heterogeneous computational elements and an interconnection network.

Toi discloses an imaging system with a single FPGA 106 that may be configured for different imaging functions. The Office Action concedes that Toi does not disclose that the computational elements are heterogeneous with different fixed architectures. (p. 8). The Office Action has asserted that DeHon discloses heterogeneous computational elements. However, DeHon discloses a programmable integrated circuit that has identical intermediate-grain processing elements (basic functional units, BFUs 100) that has addressable memory and logic resources. The BFUs 100 as shown in Fig. 6 in DeHon are identical and therefore are not heterogeneous computational units as required by the claims.

The Office Action cites elements F, A, and B of Figs. 1-5 of DeHon as different controllers with different architectures. Applicant respectfully disagrees with this characterization. The elements F, A and B in Figs. 1-5 of DeHon are actually each a BFU 100

shown in Fig. 6 that are configured via control signals for a pre-determined function such as an arithmetic logic unit, a function store, F, and further instructions stores, A and B. (Col. 5, ll. 12-22). The different functions of the ALU 120 in each of the BFUs 100 in Figs. 1-5 is not a function of adaptable hardware having different architectures as each of the ALUs 120 are identical with the same pre-determined functions. DeHon explains that the ALU 120 of the basic functional unit 100 has certain operations that may be configured using an ALU function port, Fa. (Col. 6, ll. 27-65). This is the equivalent of software changing the function of a general processor. In each case, the hardware of the BFUs 100 is not reconfigured as the BFUs are adapted for different functions detailed by the Office Action by stored instructions sent to the ALU function port Fa of the respective BFU. DeHon explains that groups of BFUs may be programmed to perform various functions and that these groupings that are configured to perform the specific hardware functions. (Col. 5, ll. 6-10). However Applicant respectfully submits that this is the result of the control signals (software) to the respective ALUs of the BFUs which are all identical. The Office Action has also cited Col 11, ll. 45-49 and Col. 12, ll. 9-12 and ll. 20-25 of DeHon for controllers with different architectures. (pp. 8-9). However, these sections support Applicant's position that the controllers (BFUs 100) have identical architectures. Col. 11, ll. 45-49 describes a control architecture that is programmed, however the control architecture itself is based on an identical BFU in Fig. 9 programmed as a controller. (Col. 11, ll. 54-56). Col. 12, ll. 9-12 and ll. 20-25 describe hardware components such as an OR-plane 210 that is contained in "each of the BFUs." The BFUs may be programmed for different functions, but the fundamental architecture for each of the BFU cells 100 is identical for "the smallest logic unit from which more complex processing units can be built." (Col. 9, ll. 6-9, Fig. 9).

The Office Action has also cited a "hardwired control mechanism which is unable to be defined by a user" as allegedly supported by Col. 13, ll. 38-40 and 44-47. (p. 9). However, these mechanisms in Col. 13, ll. 38-47 relate to the configuration memory 105 having a programmable control and a fixed control which are used to then configure the interconnections between the BFU as shown in Fig. 21 and explained in Col. 6, ll. 19-23. The present claims relate to configurable hardware that are computational units. The configuration memory 105 is not a computational unit. Further, the configuration memory 105 is in each of the BFUs are identical and therefore there is only one "architecture" namely a configuration memory with both fixed and dynamic controls.

The Office Action also defines the different architectures as an element that is constructed from multiple BFUs compared with a BFU that is independent and able to be independently changed citing col. 2, ll. 43-47 and Fig 35. (p. 9). As explained above, the grouping of BFUs via the programmable interconnection network 101 as outlined in Col. 2, ll, 43-47 does not constitute different architectures because such groupings may be changed, but the computational units themselves (the BFUs) remain the same identical units. Fig. 35 also supports this point as it explains that "all datapaths are wired using static source mode" and the "ALU operations are set in static value mode." (Col. 16, ll. 25-29). The datapaths being wired relates to the user of a BFU static setting configuring the programmable interconnection network 101. The "wired" term for Fig. 35 refers to the programming of the interconnect for datapaths between the BFUs that are set for multiplication via one of the static values. The Abstract explains that "the interconnect supports three different modes of operation: a static value in which a value set by the configuration data is provided to a functional unit, static source in which another functional unit serves as the value source, and a dynamic source mode in which the

source is determined by the value from another functional unit." Thus, the grouping of identical BFUs is not an architecture because it is being configured using the interconnection network and therefore could be changed by activating a different static value or the dynamic modes from the BFU configuration memory 105.

The claims are allowable over the combination of DeHon and Toi because that combination does not disclose "heterogeneous computational units" since all of the computational units in DeHon are identical.

The Amended Claims and the Cited References

Applicant has amended claims 1, 49 and 55-56 to require that a plurality of heterogeneous computational units include a first computational unit with a first architecture having algorithmic logic for simple computations and a second digital processing architecture having algorithmic logic for digital signal processing. The amended claims are now patentable over the combination of Toi and DeHon. Such a combination does not disclose heterogeneous computational units having a simple type of architecture and a more complex architecture for digital signal processing. As explained above, the BFUs in DeHon are identical and therefore do not disclose two different types of computational units including a dedicated digital signal processing unit. The "heterogeneous" electronic circuit units described in DeHon are actually identical basic functional units (BFU) that have been programmed for different functions. The same "heterogeneous" electronic circuit elements are present in each BFU as shown in Figs. 6 and 9 of DeHon. As explained above, the computational unit level (BFU 100) in DeHon are actually similar to prior art FPGAs such as that in Toi that have computational elements that are the same for each cell. Since the FPGAs in Toi and the BFUs 100 in DeHon are identical to each

other, neither reference discloses computational units with different architectures including a first simple computational architecture and a second digital signal processing architecture as now required by the claims.

Conclusion

It is Applicant's belief that all of the claims are now in condition for allowance and actions towards that effect is respectfully requested.

If there are any matters which may be resolved or clarified through a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney at the number indicated.

Respectfully submitted,

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